Amendments to the Claims

Claim 1: (currently amended) A method of fabricating an integrated circuit, comprising the steps of:

forming a first interlevel dielectric over a semiconductor body;

forming a layer of resistor material over said first interlevel dielectric layer;

forming a metal stack on said layer of resistor material;

forming a first pattern over said metal stack;

etching said metal stack and said layer of resistor material using said first pattern to form a plurality of metal lines ~~in addition to and separate from~~ and a thin film resistor ~~area~~, wherein said metal lines are physically separated from said thin film resistor;

removing said first pattern;

forming a second pattern to expose a portion of said metal stack over ~~a~~ said thin film resistor ~~area~~;

removing said exposed portion of said metal stack ~~to form a thin film resistor~~.

Claim 2: (original) The method of claim 1, wherein said second pattern is a photoresist pattern.

Claim 3: (original) The method of claim 1, wherein said second pattern is a hardmask.

Claim 4: (previously presented) The method of claim 3, wherein said step of forming said second pattern comprises the steps of:

forming a hardmask layer over said metal stack;

forming a photoresist pattern over said hardmask layer to expose a portion of said hardmask layer over the thin film resistor area.;

removing said exposed portion of said hardmask layer; and

removing said photoresist pattern.

Claim 5: (original) The method of claim 4, wherein said hardmask layer comprises silicon dioxide.

Claim 6: (original) The method of claim 1, wherein said interlevel dielectric layer comprises vias formed at a surface thereof.

Claim 7: (original) The method of claim 1, wherein a portion of said metal stack remains at a first end and a second end of said thin film resistor.

Claim 8: (cancelled).

Claim 9: (currently amended) The method of claim 16 ~~8~~, wherein said second pattern is a photoresist pattern.

Claim 10: (currently amended) The method of claim 16 ~~8~~, wherein said second pattern is a hardmask.

Claim 11: (previously presented) The method of claim 10, wherein said step of forming said second pattern comprises the steps of:

forming a hardmask layer over said metal stack;

forming a photoresist pattern over said hardmask layer to expose a portion of said hardmask layer over the thin film resistor area.;

removing said exposed portion of said hardmask layer; and

removing said photoresist pattern.

Claim 12: (currently amended) The method of claim 16 ~~8~~, wherein said first interlevel dielectric layer comprises vias formed at a surface thereof.

Claim 13: (currently amended) The method of claim 16 ~~8~~, wherein a portion of said metal stack remains at a first end and a second end of said thin film resistor.

Claims 14-15: (cancelled).

Claim 16 (new): A method of fabricating an integrated circuit, comprising the steps of:

providing a semiconductor body having a first interlevel dielectric layer;

forming a layer of resistor material over said first interlevel dielectric layer;

forming a metal stack on said layer of resistor material;

forming a first pattern over said metal stack, said first pattern covering said metal stack;

dry etching said metal stack and said layer of resistor material using said first pattern to form at least one metal line and a thin film resistor, wherein said at least one metal line is physically separated from said thin film resistor;

removing said first pattern;

forming a second pattern to expose a portion of said metal stack over said thin film resistor;

removing said exposed portion of said metal stack using a wet etch;

removing said second pattern; and

forming a second interlevel dielectric layer over said at least one metal line and said thin film resistor.